

EMIF03-SIM02F3

3-line IPAD™, EMI filter including ESD protection

Features

- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- Lead-free package
- Very low PCB space consuming: 1.2 mm²
- Very thin package: 0.60 mm
- High efficiency in ESD suppression
- High reliability offered by monolithic integration
- High reduction of parasitic elements through integration and wafer level packaging

Complies with the following standards

- IEC 61000-4-2 Level 4 on external and V_{cc} pins:
 - 15 kV (air discharge)
 - 8 kV (contact discharge)
- IEC 61000-4-2 Level 1on internal pins:
 - 2 kV (air discharge)
 - 2 kV (contact discharge)
- MIL STD 883E Method 3015-6 Class 3

Applications

EMI filtering and ESD protection for:

- SIM Interface (subscriber identify module)
- UIM Interface (universal identify module)

Description

The EMIF03-SIM02F3 is a highly integrated device designed to suppress EMI / RFI noise in all systems subjected to electromagnetic interferences.

This filter includes an ESD protection circuitry which prevents damage to the application when subjected to ESD surges up to 15 kV.

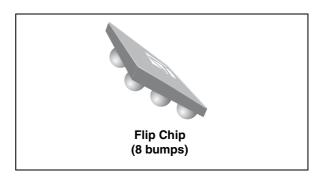


Figure 1. Pin configuration (bump side)

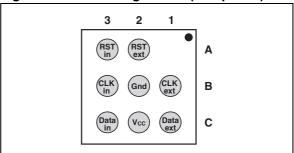
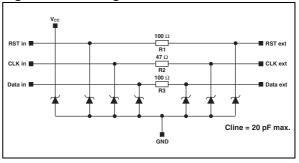


Figure 2. Configuration



TM: IPAD is a trademark of STMicroelectronics.

Electrical characteristics EMIF03-SIM02F3

1 Electrical characteristics

Table 1. Absolute maximum ratings ($T_{amb} = 25$ °C)

| Symbol | Parameter and test conditions | Value | Unit |
|------------------|------------------------------------------------|------------|------|
| | Internal pins (A3, B3, C3): | | |
| V _{PP} | ESD discharge IEC 61000-4-2, air discharge | 2 | |
| | ESD discharge IEC 61000-4-2, contact discharge | 2 | kV |
| | External pins (A2, B1, C2, C1): | | KV |
| | ESD discharge IEC 61000-4-2, air discharge | 15 | |
| | ESD discharge IEC 61000-4-2, contact discharge | 8 | |
| Tj | Maximum junction temperature | 125 | °C |
| T _{op} | Operating temperature range | -40 to +85 | °C |
| T _{stg} | Storage temperature range | -55 to 150 | °C |

Figure 3. Electrical characteristics (definitions)

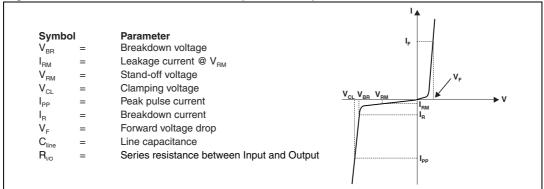


Table 2. Electrical characteristics ($T_{amb} = 25$ °C)

| Symbol | Test conditions | Min. | Тур. | Max. | Unit |
|--------------------------------|----------------------------------------------------------------------|------|------|------|------|
| V_{BR} | I _R = 1 mA | 6 | - | 20 | V |
| I _{RM} | V _{RM} = 3 V | - | 1 | 0.2 | μΑ |
| R_d | | - | 1.5 | - | Ω |
| R _{1,} R ₃ | Tolerance ± 20% | - | 100 | - | Ω |
| R ₂ | Tolerance ± 20% | - | 47 | - | Ω |
| C _{line} | $V_{line} = 0 \text{ V}, V_{osc} = 30 \text{ mV}, F = 1 \text{ MHz}$ | - | • | 20 | pF |

Figure 4. S21 (dB) attenuation measurement Figure 5. S21 (dB) attenuation measurement (A2-A3 line) S21 (dB) attenuation measurement (B1-B3 line)

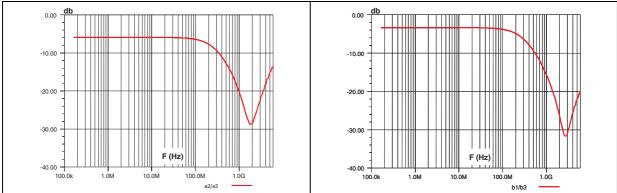


Figure 6. S21 (dB) attenuation measurement Figure 7. Analog crosstalk measurements (C1-C3 line)

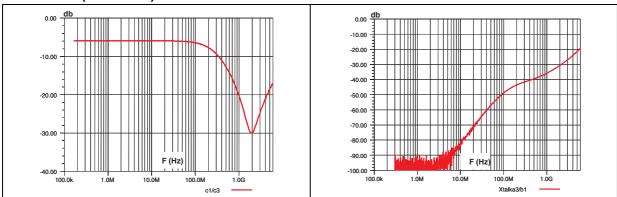
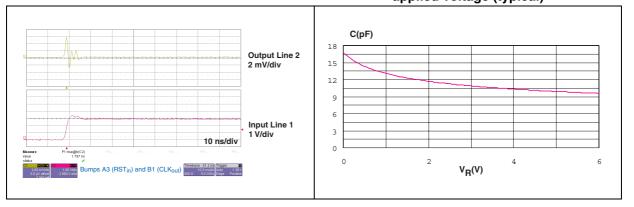


Figure 8. Digital crosstalk measurements

Figure 9. Line capacitance versus reverse applied voltage (typical)



Aplac model EMIF03-SIM02F3

2 Aplac model

Figure 10. Aplac model

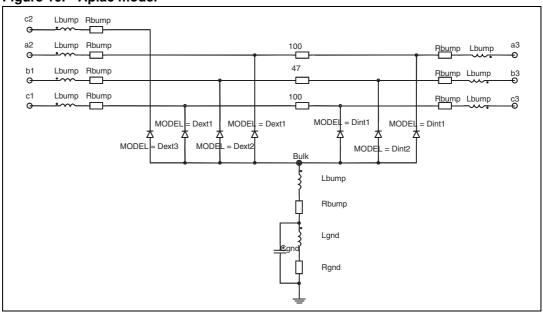


Figure 11. Aplac parameters

| aplacvar Rs 150m | Dint1 | Dext1 | Dint2 | Dext2 | Dext3 |
|----------------------|-----------|-----------|-----------|-----------|----------|
| aplacvar Cext1 12pF | BV=15 | BV=15 | BV=15 | BV=15 | BV=15 |
| | | 20 | | | |
| aplacvar Cext2 14pF | CJO=Cint1 | CJO=Cext1 | CJO=Cint2 | CJO=Cext2 | CJO=Cext |
| aplacvar Cext3 18pF | IBV=1u | IBV=1u | IBV=1u | IBV=1u | IBV=1u |
| aplacvar Cint1 4.5pF | IKF=1000 | IKF=1000 | IKF=1000 | IKF=1000 | IKF=1000 |
| aplacvar Cint2 4pF | IS=10f | IS=10f | IS=10f | IS=10f | IS=10f |
| aplacvar Rbump 17m | ISR=100p | ISR=100p | ISR=100p | ISR=100p | ISR=100p |
| aplacvar Lbump 43pH | N=1 | N=1 | N=1 | N=1 | N=1 |
| aplacvar Rgnd 500m | M=0.3333 | M=0.3333 | M=0.3333 | M=0.3333 | M=0.3333 |
| aplacvar Lgnd 50pH | RS=0.29 | RS=0.25 | RS=0.31 | RS=0.28 | RS=0.25 |
| aplacvar Cgnd 0.15pF | VJ=0.6 | VJ=0.6 | VJ=0.6 | VJ=0.6 | VJ=0.6 |
| aplacvar Rsub 100m | TT=50n | TT=50n | TT=50n | TT=50n | TT=50n |

EMIF03-SIM02F3 Aplac model

Figure 12. Voltages when IEC 61000-4-2 (+15 kV air discharge) applied to external pin

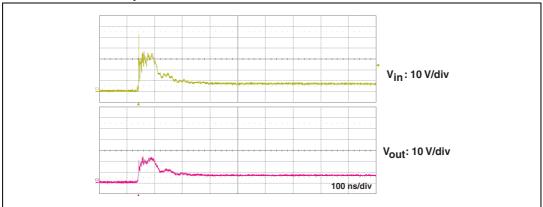
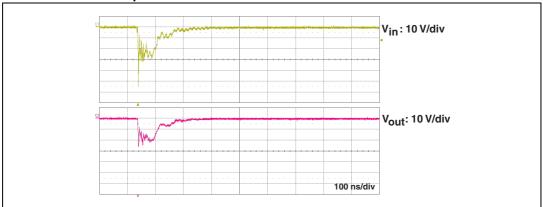
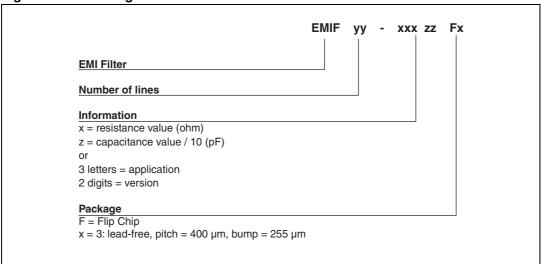


Figure 13. Voltages when IEC 61000-4-2 (- 15 kV air discharge) applied to external pin



3 Ordering information scheme

Figure 14. Ordering information scheme



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 15. Package dimensions

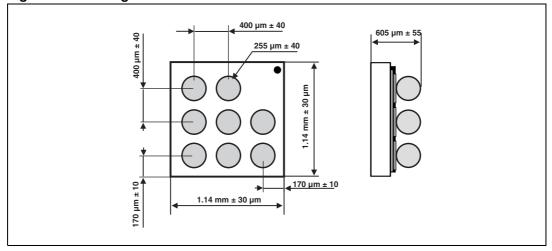


Figure 16. Footprint

Figure 17. Marking

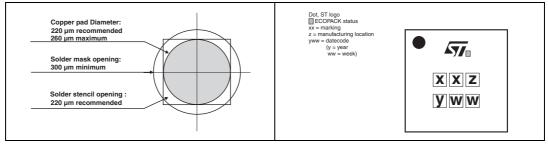
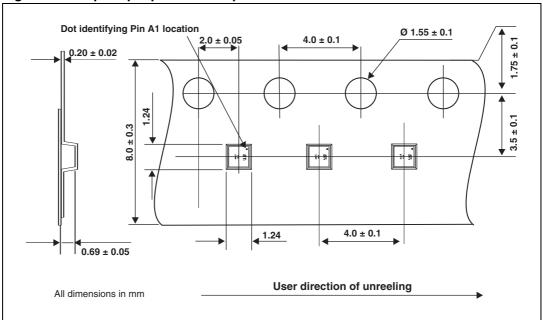


Figure 18. Flip Chip tape and reel specification



Ordering information 5

Ordering information Table 3.

| Order code | Marking | Package | Weight | Base qty | Delivery mode |
|----------------|---------|-----------|---------|----------|------------------|
| EMIF03-SIM02F3 | НА | Flip Chip | 1.74 mg | 5000 | Tape and reel 7" |

Note:

More information is available in the application notes:

AN2348: "STMicroelectronics 400 micro-metre Flip Chip: package description and

recommendation for use"

AN1751: "EMI filters: recommendations and measurements"

Revision history EMIF03-SIM02F3

6 Revision history

Table 4. Document revision history

| Date | Revision | Changes |
|-------------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19-Jul-2005 | 1 | Initial release. |
| 26-Feb-2007 | 2 | Changed out to ext in Configuration diagram on page 1. Added Ecopack statement. Reformatted to current layour standard. Updated Application note AN2348 reference and description. |
| 28-Nov-2007 | 3 | Updated ECOPACK statement. Updated Figure 14, Figure 15, Figure 16 and Figure 18. Reformatted to current standards. |
| 09-Feb-2010 | 4 | Updated die dimensions in <i>Figure 15</i> and pocket dimensions in <i>Figure 18</i> . |
| 07-Apr-2010 | 5 | Updated tolerance dimensions in Figure 15: Package dimensions. |

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